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Abstract
Audio, music and image are the most basic means of adult human communications. As technology advances, more and more useful audio tools become available. Hence, researchers can study audio more efficiently and invent new ways of audio processing for the benefits of humankind. Most audio compression systems in the markets are implemented with high-price hardware modules or with higher audio distortion. The main purpose of this thesis is to develop a real-time low-complexity low-loss audio compression algorithm. The techniques of noise shaped quantiser and ADPCM algorithm[7-8] are employed to develop our algorithm. Simulation results show that the algorithm can achieve excellent results with low cost.

The proposed architecture has been verified by using Verilog HDL. Then, we employed Synopsys Design Compiler to synthesize the design with the standard-cell from TSMC's 0.35um cell library. Finally, the layout for the design was generated with the Avant! tools, Apollo (for floorplan, placement and routing), and Dracula (for DRC, ERC and LVS checks). The total area of it is about 1818.6um*1819.5um and the gate count is about 5252.The hardware architecture is also implemented on an Altera EPF10K50EQC240-3 FPGA chip. A audio compression system is built by integrating the chip with an 8051 microprocessor to verify the performance of our architecture.
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